

**REMARKS**

Claims 1 to 3, 5 to 12 and 15 to 23 were previously pending. Claims 1, 2, 5 to 11, 15 to 17, and 19 to 23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 5,481,563 (Hamre) in view of United States Patents Nos. 4,974,234 (Brandt) and 5,550,860 (Georgiou). Claims 3, 12 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Hamre in view of Brandt, Georgiou and United States Patent No. 6,100,724 (Yoshimura).

The newly cited Georgiou reference relates to a transceiver employing a digital phase alignment technique used for jitter and noise filtering, but does not disclose or even infer the measurement of jitter, as in the present invention. Figure 1 of the Georgiou reference relates to a conventional phase-alignment circuit arrangement in which an input signal is compared to a sampling clock signal in an attempt to synchronize the two signals. Since the description of Figure 1 does not contain any reference to the measurement of jitter, Applicant respectfully submits that the use of a single clock signal for phase alignment does not suggest that the same can be used in the measurement of jitter, as in the present invention. Accordingly, there is no motivation to take the clock signal from the Georgiou reference and compare it to the data signal in the Hamre et al reference, as the Georgiou et al reference relates to phase alignment, while the Hamre disclosure relies on a comparison of two clock signals for jitter measurement.

Similarly, the invention disclosed in the Georgiou reference, as illustrated in Figure 2, does not disclose the use of a single clock signal for measuring jitter, and in fact discloses the use of a sampling clock signal and a reference clock signal, both of which are input the logic 32, for compensating the input signal. Accordingly, the embodiment of Figure 2 is not only unrelated to jitter measurement, but also discloses the use of two clock signals for phase alignment, in contrast to the present invention.

Neither embodiment discloses or even infers the desire or the ability to eliminate one of the clock signals and the required signal generator by counting when the number of sampling times in any bit of the digital signal is different from a predetermined number.

As previously stated, the system disclosed in the Hamre reference uses two clock signals, i.e. a nominal clock and an early clock, both of which are derived from the data signal and would still contain some jitter, which may not matter since the results of the early clock are compared to those of the nominal clock. As a result, only a positive jitter peak can be established based on a statistical error rate performance of the early clock relative to the nominal clock.

The present invention eliminates the need for both the nominal and early clock signals by counting the number of pulses from only a single "offset", "jitter-free" reference clock signal that fall in each bit of the digital signal, and comparing that count to a predetermined number that would occur if there was no jitter. Then the number of times, when the number of sampling times in any bit of the digital signal

is different from the predetermined number, is counted, and from this count the jitter is determined.

The clock signal according to the present invention is "offset" from the data signal, not just another clock signal, i.e. the delayed clock signal, as in the Hamre reference. In the present invention, the combination of offsetting and making the reference clock signal jitter free enable a single clock signal to provide: *occasions when the number of sampling times in any bit of said digital signal is different from the predetermined number*, whereby the number of occasions derived from the single reference clock signal are used to provide both low and high frequency jitter measurements.

The present invention is much simpler than the device disclosed in the Hamre reference, i.e. does not require the hardware to generate both the nominal and early clock signals, and enables the recovery of both a positive and negative peak by looking for any errors, not just statistical error rate information.

Accordingly, Applicant respectfully disagrees that the combination of the Hamre reference, disclosing the use of two independently generated clock signals, and the Georgiou reference, disclosing a phase alignment technique, will result in the present invention, which requires only a signal self-generated clock signal for jitter measurement.

As such, it is respectfully submitted that all of the claims remaining in the application are in condition for allowance. Early and favorable consideration would be appreciated.

In re Patent Application of:  
**BREWER ET AL.**  
Serial No. **09/674,444**  
Filed: **OCTOBER 31, 2000**

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Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 50-1465 and please credit any excess fees to such deposit account.

Respectfully submitted,



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